REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-19 are remain in the application. Claims 12, 13, and 16-19 are subject to examination and claims 1-11, 14, and 15 have been withdrawn from examination. Claim 12 has been amended.

In the second item under "Claim Rejections - 35 USC § 102" on page 2 of the above-identified Office Action, claims 12-13, and 16-19 have been rejected as being anticipated by Gambino et al. (EP 0967643 A2) (hereinafter " Gambino") under 35 U.S.C. § 102(a).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 8, lines 10-12, page 20, lines 8-9, page 22, line 26 to page 24, line 8 of the specification as well as the drawings of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method for fabricating a

trench capacitor, which has the following sequential order of steps:

etching a trench into a main surface of a silicon substrate;

producing covered silicon regions by applying a covering material to regions of the trench on which a lower, metallic capacitor electrode should not be formed;

forming the lower, metallic capacitor electrode in a self-aligned manner by selectively forming a metal silicide on uncovered silicon regions such that the capacitor is at least partially configured in the trench and the lower, metallic capacitor electrode adjoins a wall of the trench; and

after forming the lower, metallic capacitor electrode, providing a storage dielectric on the lower, metallic capacitor electrode and providing an upper capacitor electrode on the storage dielectric.

According to claim 12 the lower capacitor electrode of the capacitor is formed first (by self-aligned silicidation) and the capacitor dielectric is formed subsequently.

Claim 12 recites a method which achieves formation of a first capacitor electrode having improved electrical conductivity compared to prior art capacitors. The capacitance of an integrated capacitor increases with reduced thickness of the capacitor dielectric. Furthermore, capacitance increases with the amount of electrical charges which accumulate directly adjacent to the capacitor dielectric. According to the present invention a silicide layer is formed on the surface of that capacitor electrode which is formed first (that is prior to formation of the capacitor dielectric). **Because the silicide layer forms the lower electrode in the trench, the amount of electrical charges storable in the silicide layer is larger that in case of a conventional lower electrode not having a silicide laver. Furthermore. since the capacitor dielectric is formed directly on the silicide laver (which forms the lower electrode as recited in the last paragraph of claim 12), the amount of electrical charges storable directly adjacent the capacitor dielectric is increased compared to prior art capacitors** which do not contain a silicide layer in direct contact with the capacitor dielectric. Thus, by depositing the capacitor dielectric on the silicide layer, the present claimed invention solves the problem of increasing the capacitance of the integrated capacitor.

The Examiner erroneously believes that Gambino shows the

present claimed invention. Applicants respectfully disagree as stated below.

Gambino does not show the method of claim 12 of the instant application and moreover, doe snot disclose or suggest the problem underlying and addressed by the present claimed invention. According to Gambino a substrate having a trench with an electrode in a broad lower trench region and also having a capacitor dielectric (see column 2, line 5, "dielectric lining") is provided which is apparent from step a) described in lines 1-6 of column 2 of Gambino. Subsequently, the trench is filled with a polysilicon layer deposited on the dielectric lining. However, the trench is not filled completely. Instead. a void is maintained in the broad lower region as disclosed in line 7 of column 2. Thus, only an outer region of the inner capacitor electrode of a trench capacitor is formed. Subsequently, according to step d) the polysilicon is removed from the outer substrate surface and from an upper, narrow trench region as disclosed in steps c) and d) in lines 8-11 of column 2 of Gambino.

At this point, the capacitor dielectric and both electrodes (at least their portions directly adjacent to the capacitor dielectric) are already completed. The sequence of steps then proceeds with step e) disclosing that a conformal refractory

metal layer is formed on the inner surface of the void in the trench ("in said narrow upper region and said broad lower region"; lines 11-13) and with step f) disclosing that the structure is annealed, thereby forming a metal silicide layer (line 14). After removing the conformal refractory metal layer in step g), the void is filled with polysilicon according to step h) as disclosed in column 2, line 17 of Gambino.

Thus, it is apparent that **Gambino only discloses forming a metal silicide laver within the inner capacitor electrode** which also is apparent from the drawings of Gambino. For example, Figure 2 illustrates the outer electrode 18, the capacitor dielectric 20, the inner capacitor electrode 26, 32, 34, and the silicide layer 32 which is formed between an outer region 26 of the inner capacitor electrode and an inner region 34 of the inner capacitor electrode. There is no metal silicide which is located adjacent to the capacitor dielectric 20. Therefore, in Gambino the metal silicide laver does not increase the capacitance of the capacitor.

It is apparent from Gambino's Abstract, that the silicide-containing trench electrode 26, 32, 34 only serves to reduce the series resistance of the inner capacitor electrode and to reduce cell access time. The object of increasing the

capacitance is not addressed or suggested in anyway in Gambino.

Furthermore, according to the present claimed invention the metal silicide is formed first and the capacitor dielectric is deposited thereon subsequently. According to Gambino, however, the capacitor dielectric 20 is formed first and the metal silicide 32 is formed later. It is not formed directly on the dielectric 20 and according to the teachings of Gambino it is not possible to form the metal silicide directly on the dielectric 20 since the metal silicide can only be formed in self-aligned manner on those exposed surface regions consisting of silicon. The capacitor dielectric 20, however, is not silicon or polysilicon. Therefore, it would not be possible, even if departing from the explicit teaching of Gambino, to achieve formation of the metal silicide directly on the capacitor dielectric 20 and to increase the capacitance of the capacitor as achieved according to the present claimed invention.

Accordingly, Gambino fails to provide any suggestion of the method of claim 12 and, though disclosing a silicide layer formed in self-aligned manner, Gambino fails to show any indication of how to increase the capacitance of an integrated capacitor which is achieved by the method recited in claim 12.

For these reasons claims 12, 13 and 16-19 are considered patentable over Gambino.

Gambino does not show "fabricating a trench capacitor, which comprises the following sequential order of steps" and "after forming the lower, metallic capacitor electrode, providing a storage dielectric on the lower, metallic capacitor electrode and providing an upper capacitor electrode on the storage dielectric" as recited in claim 12 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 12. Claim 12 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 12.

In view of the foregoing, reconsideration and allowance of claims 12, 13, and 16-19 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Appl. No. 10/650,055
Amdt. dated 6/6/05
Reply to Office action of 2/9/05

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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FDP/bb

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